

	L #	Hits	Search Text	DBs
1	L2	16698	vector near10 (gather\$3 scatter\$3 stor\$3)	USPAT; US-PGPUB
2	L3	18595	address near10 ((start\$3 begin\$4 first max\$4) near20 (last finish\$3 end\$3 min\$4))	USPAT; US-PGPUB
3	L4	1864	2 near20 (3 area range limit space bound\$3)	USPAT; US-PGPUB
4	L5	105015	address near10 (load\$3 read\$3 fetch\$3 (memory near5 access\$3))	USPAT; US-PGPUB
5	L7	10914	(overlap\$4 cover\$3 coincid\$3 match\$3 compar\$3) near20 5	USPAT; US-PGPUB
6	L9	44	(vector near20 (gather\$3 scatter\$3)).ab,ti.	USPAT; US-PGPUB
7	L8	102	4 and 7	USPAT; US-PGPUB
8	L11	6479	vector near10 (gather\$3 scatter\$3 stor\$3)	EPO; JPO; DERWENT; IBM_TDB
9	L12	3365	address near10 ((start\$3 begin\$4 first max\$4) near20 (last finish\$3 end\$3 min\$4))	EPO; JPO; DERWENT; IBM_TDB
10	L13	632	11 near20 (12 area range limit space bound\$3)	EPO; JPO; DERWENT; IBM_TDB
11	L14	63880	address near10 (load\$3 read\$3 fetch\$3 (memory near5 access\$3))	EPO; JPO; DERWENT; IBM_TDB
12	L15	4813	(overlap\$4 cover\$3 coincid\$3 match\$3 compar\$3) near20 14	EPO; JPO; DERWENT; IBM_TDB
13	L16	15	13 and 15	EPO; JPO; DERWENT; IBM_TDB
14	L19	13	(vector and instruction and (gather\$3 scatter\$3)).ab,ti.	EPO; JPO; DERWENT; IBM_TDB
15	L20	4	(vector and instruction and (gather\$3 scatter\$3)).ab,ti.	USPAT; US-PGPUB

	Docu ment ID	U	Title	Current OR
1	US 20030 18811 1 A1	<input type="checkbox"/>	Method and apparatus for satisfying load operations	711/154
2	US 20030 18781 4 A1	<input checked="" type="checkbox"/>	Parallel search technique	707/1
3	US 65534 82 B1	<input checked="" type="checkbox"/>	Universal dependency vector/queue entry	712/216
4	US 63082 59 B1	<input checked="" type="checkbox"/>	Instruction queue evaluating dependency vector in portions during different clock phases	712/214
5	US 62126 23 B1	<input checked="" type="checkbox"/>	Universal dependency vector/queue entry	712/216
6	US 62126 22 B1	<input checked="" type="checkbox"/>	Mechanism for load block on store address generation	712/216
7	US 61417 47 A	<input checked="" type="checkbox"/>	System for store to load forwarding of individual bytes from separate store buffer entries to form a single load word	712/225
8	US 61227 27 A	<input checked="" type="checkbox"/>	Symmetrical instructions queue for high clock frequency scheduling	712/214
9	US 60584 65 A	<input checked="" type="checkbox"/>	Single-instruction-multiple-data processing in a multimedia signal processor	712/7
10	US 59251 45 A	<input checked="" type="checkbox"/>	Integrated circuit tester with cached vector memories	714/738
11	US 58944 84 A	<input checked="" type="checkbox"/>	Integrated circuit tester with distributed instruction processing	714/738
12	US 58813 07 A	<input checked="" type="checkbox"/>	Deferred store data read with simple anti-dependency pipeline inter-lock control in superscalar processor	712/23
13	US 58784 24 A	<input checked="" type="checkbox"/>	Method and apparatus for indexing patterned sparse arrays for microprocessor data cache	707/102
14	US 58386 94 A	<input checked="" type="checkbox"/>	Dual source data distribution system for integrated circuit tester	714/738
15	US 58095 52 A	<input checked="" type="checkbox"/>	Data processing system, memory access device and method including selecting the number of pipeline stages based on pipeline conditions	711/169
16	US 58056 10 A	<input checked="" type="checkbox"/>	Virtual channel data distribution system for integrated circuit tester	714/738
17	US 57245 48 A	<input checked="" type="checkbox"/>	System including processor and cache memory and method of controlling the cache memory	711/138
18	US 55817 21 A	<input checked="" type="checkbox"/>	Data processing unit which can access more registers than the registers indicated by the register fields in an instruction	712/200
19	US 54993 50 A	<input checked="" type="checkbox"/>	Vector data processing system with instruction synchronization	712/220
20	US 54308 88 A	<input checked="" type="checkbox"/>	Pipeline utilizing an integral cache for transferring data to and from a register	711/205
21	US 53496 92 A	<input checked="" type="checkbox"/>	Instruction handling sequence control system for simultaneous execution of vector instructions	712/9
22	US 53234 89 A	<input checked="" type="checkbox"/>	Method and apparatus employing lookahead to reduce memory bank contention for decoupled operand references	711/167

	Docum ent ID	U	Title	Current OR
23	US 52476 35 A	<input checked="" type="checkbox"/>	Vector processing system for invalidating scalar cache memory block indicated by address in tentative vector store instruction	711/3
24	US 52416 33 A	<input checked="" type="checkbox"/>	Instruction handling sequence control system for simultaneous execution of instructions	712/216
25	US 51485 36 A	<input checked="" type="checkbox"/>	Pipeline having an integral cache which processes cache misses and loads data in parallel	711/140
26	US 48736 30 A	<input checked="" type="checkbox"/>	Scientific processor to support a host processor referencing common memory	712/3
27	US 48705 69 A	<input type="checkbox"/>	Vector access control system	711/151

	Docum ent ID	U	Title	Current OR
1	US 20030 18811 1 A1	<input type="checkbox"/>	Method and apparatus for satisfying load operations	711/154
2	US 20030 03722 1 A1	<input type="checkbox"/>	Processor implementation having unified scalar and SIMD datapath	712/3
3	US 60584 65 A	<input type="checkbox"/>	Single-instruction-multiple-data processing in a multimedia signal processor	712/7
4	US 59305 07 A	<input type="checkbox"/>	Compiling processing apparatus	717/160
5	US 58955 01 A	<input type="checkbox"/>	Virtual memory system for vector based computer systems	711/207
6	US 58389 84 A	<input type="checkbox"/>	Single-instruction-multiple-data processing using multiple banks of vector registers	712/5
7	US 58095 52 A	<input type="checkbox"/>	Data processing system, memory access device and method including selecting the number of pipeline stages based on pipeline conditions	711/169
8	US 54189 73 A	<input type="checkbox"/>	Digital computer system with cache controller coordinating both vector and scalar operations	712/3
9	US 53496 92 A	<input type="checkbox"/>	Instruction handling sequence control system for simultaneous execution of vector instructions	712/9
10	US 53197 91 A	<input type="checkbox"/>	System for predicting memory fault in vector processor by sensing indication signal to scalar processor to continue a next vector instruction issuance	712/3
11	US 52476 35 A	<input type="checkbox"/>	Vector processing system for invalidating scalar cache memory block indicated by address in tentative vector store instruction	711/3
12	US 52416 33 A	<input type="checkbox"/>	Instruction handling sequence control system for simultaneous execution of instructions	712/216
13	US 51796 74 A	<input type="checkbox"/>	Method and apparatus for predicting valid performance of virtual-address to physical-address translations	711/204
14	US 48736 30 A	<input type="checkbox"/>	Scientific processor to support a host processor referencing common memory	712/3
15	US 48581 15 A	<input type="checkbox"/>	Loop control mechanism for scientific processor	712/7
16	US 47220 49 A	<input type="checkbox"/>	Apparatus for out-of-order program execution	712/3
17	US 45946 82 A	<input type="checkbox"/>	Vector processing	712/6

	L #	Hits	Search Text	DBs
1	L2	16698	vector near10 (gather\$3 scatter\$3 stor\$3)	USPAT; US-PGPUB
2	L3	18595	address near10 ((start\$3 begin\$4 first max\$4) near20 (last finish\$3 end\$3 min\$4))	USPAT; US-PGPUB
3	L4	1864	2 near20 (3 area range limit space bound\$3)	USPAT; US-PGPUB
4	L5	105015	address near10 (load\$3 read\$3 fetch\$3 (memory near5 access\$3))	USPAT; US-PGPUB
5	L7	10914	(overlap\$4 cover\$3 coincid\$3 match\$3 compar\$3) near20 5	USPAT; US-PGPUB
6	L9	44	(vector near20 (gather\$3 scatter\$3)).ab,ti.	USPAT; US-PGPUB
7	L8	102	4 and 7	USPAT; US-PGPUB
8	L11	6479	vector near10 (gather\$3 scatter\$3 stor\$3)	EPO; JPO; DERWENT; IBM_TDB
9	L12	3365	address near10 ((start\$3 begin\$4 first max\$4) near20 (last finish\$3 end\$3 min\$4))	EPO; JPO; DERWENT; IBM_TDB
10	L13	632	11 near20 (12 area range limit space bound\$3)	EPO; JPO; DERWENT; IBM_TDB
11	L14	63880	address near10 (load\$3 read\$3 fetch\$3 (memory near5 access\$3))	EPO; JPO; DERWENT; IBM_TDB
12	L15	4813	(overlap\$4 cover\$3 coincid\$3 match\$3 compar\$3) near20 14	EPO; JPO; DERWENT; IBM_TDB
13	L16	15	13 and 15	EPO; JPO; DERWENT; IBM_TDB
14	L19	13	(vector and instruction and (gather\$3 scatter\$3)).ab,ti	EPO; JPO; DERWENT; IBM_TDB
15	L20	4	(vector and instruction and (gather\$3 scatter\$3)).ab,ti.	USPAT; US-PGPUB
16	L22	1	(overlap\$4 cover\$3 coincid\$4 match\$3 compar\$3) near20 14 and 13 not 16	EPO; JPO; DERWENT; IBM_TDB
17	L21	1	(overlap\$4 cover\$3 coincid\$4 match\$3 compar\$3) near20 5 and 4 not 8	USPAT; US-PGPUB
18	L24	254	vector near5 (gather scatter store) near20 load	USPAT; US-PGPUB
19	L25	8	vector near5 (gather scatter) near20 load	USPAT; US-PGPUB
20	L28	7	(overlap\$4 cover\$3 coincid\$3 match\$3 compar\$3) near20 address near99 24	USPAT; US-PGPUB
21	L29	17	24 near99 (3 area range limit space bound\$3)	USPAT; US-PGPUB
22	L30	27	(overlap\$4 cover\$3 coincid\$3 match\$3 compar\$3) near20 load near10 address and 24	USPAT; US-PGPUB

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1	L2	16698	vector near10 (gather\$3 scatter\$3 stor\$3)	USPAT; US-PGPUB
2	L3	18595	address near10 ((start\$3 begin\$4 first max\$4) near20 (last finish\$3 end\$3 min\$4))	USPAT; US-PGPUB
3	L4	1864	2 near20 (3 area range limit space bound\$3)	USPAT; US-PGPUB
4	L5	105015	address near10 (load\$3 read\$3 fetch\$3 (memory near5 access\$3))	USPAT; US-PGPUB
5	L7	10914	(overlap\$4 cover\$3 coincid\$3 match\$3 compar\$3) near20 5	USPAT; US-PGPUB
6	L9	44	(vector near20 (gather\$3 scatter\$3)).ab,ti.	USPAT; US-PGPUB
7	L8	102	4 and 7	USPAT; US-PGPUB
8	L11	6479	vector near10 (gather\$3 scatter\$3 stor\$3)	EPO; JPO; DERWENT; IBM_TDB
9	L12	3365	address near10 ((start\$3 begin\$4 first max\$4) near20 (last finish\$3 end\$3 min\$4))	EPO; JPO; DERWENT; IBM_TDB
10	L13	632	11 near20 (12 area range limit space bound\$3)	EPO; JPO; DERWENT; IBM_TDB
11	L14	63880	address near10 (load\$3 read\$3 fetch\$3 (memory near5 access\$3))	EPO; JPO; DERWENT; IBM_TDB
12	L15	4813	(overlap\$4 cover\$3 coincid\$3 match\$3 compar\$3) near20 14	EPO; JPO; DERWENT; IBM_TDB
13	L16	15	13 and 15	EPO; JPO; DERWENT; IBM_TDB
14	L19	13	(vector and instruction and (gather\$3 scatter\$3)).ab,ti.	EPO; JPO; DERWENT; IBM_TDB
15	L20	4	(vector and instruction and (gather\$3 scatter\$3)).ab,ti.	USPAT; US-PGPUB
16	L22	1	(overlap\$4 cover\$3 coincid\$4 match\$3 compar\$3) near20 14 and 13 not 16	EPO; JPO; DERWENT; IBM_TDB
17	L21	1	(overlap\$4 cover\$3 coincid\$4 match\$3 compar\$3) near20 5 and 4 not 8	USPAT; US-PGPUB
18	L24	254	vector near5 (gather scatter store) near20 load	USPAT; US-PGPUB
19	L25	8	vector near5 (gather scatter) near20 load	USPAT; US-PGPUB
20	L28	7	(overlap\$4 cover\$3 coincid\$3 match\$3 compar\$3) near20 address near99 24	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	US 20020 00744 9 A1	<input type="checkbox"/>	Vector scatter instruction control circuit and vector architecture information processing equipment	712/4
2	US 61191 98 A	<input checked="" type="checkbox"/>	Recursive address centrifuge for distributed memory massively parallel processing systems	711/5
3	US 57651 81 A	<input checked="" type="checkbox"/>	System and method of addressing distributed memory within a massively parallel processing system	711/5
4	US 56969 22 A	<input checked="" type="checkbox"/>	Recursive address centrifuge for distributed memory massively parallel processing systems	711/5
5	US 56896 53 A	<input checked="" type="checkbox"/>	Vector memory operations	712/222
6	US 54189 73 A	<input checked="" type="checkbox"/>	Digital computer system with cache controller coordinating both vector and scalar operations	712/3
7	US 51013 71 A	<input checked="" type="checkbox"/>	Apparatus for performing a bit serial orthogonal transformation instruction	708/520
8	US 50438 86 A	<input checked="" type="checkbox"/>	Load/store with write-intent for write-back caches	711/143

	Docum ent ID	U	Title	Current OR
1	US 20030 18811 1 A1	<input type="checkbox"/>	Method and apparatus for satisfying load operations	711/154
2	US 20030 18781 4 A1	<input type="checkbox"/>	Parallel search technique	707/1
3	US 61417 47 A	<input type="checkbox"/>	System for store to load forwarding of individual bytes from separate store buffer entries to form a single load word	712/225
4	US 57245 48 A	<input type="checkbox"/>	System including processor and cache memory and method of controlling the cache memory	711/138
5	US 53496 92 A	<input type="checkbox"/>	Instruction handling sequence control system for simultaneous execution of vector instructions	712/9
6	US 52476 35 A	<input type="checkbox"/>	Vector processing system for invalidating scalar cache memory block indicated by address in tentative vector store instruction	711/3
7	US 52416 33 A	<input type="checkbox"/>	Instruction handling sequence control system for simultaneous execution of instructions	712/216



	L #	Hits	Search Text	DBs
1	L2	16698	vector near10 (gather\$3 scatter\$3 stor\$3)	USPAT; US-PGPUB
2	L3	18595	address near10 ((start\$3 begin\$4 first max\$4) near20 (last finish\$3 end\$3 min\$4))	USPAT; US-PGPUB
3	L4	1864	2 near20 (3 area range limit space bound\$3)	USPAT; US-PGPUB
4	L5	105015	address near10 (load\$3 read\$3 fetch\$3 (memory near5 access\$3))	USPAT; US-PGPUB
5	L7	10914	(overlap\$4 cover\$3 coincid\$3 match\$3 compar\$3) near20 5	USPAT; US-PGPUB
6	L9	44	(vector near20 (gather\$3 scatter\$3)).ab,ti.	USPAT; US-PGPUB
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8	L11	6479	vector near10 (gather\$3 scatter\$3 stor\$3)	EPO; JPO; DERWENT; IBM_TDB
9	L12	3365	address near10 ((start\$3 begin\$4 first max\$4) near20 (last finish\$3 end\$3 min\$4))	EPO; JPO; DERWENT; IBM_TDB
10	L13	632	11 near20 (12 area range limit space bound\$3)	EPO; JPO; DERWENT; IBM_TDB
11	L14	63880	address near10 (load\$3 read\$3 fetch\$3 (memory near5 access\$3))	EPO; JPO; DERWENT; IBM_TDB
12	L15	4813	(overlap\$4 cover\$3 coincid\$3 match\$3 compar\$3) near20 14	EPO; JPO; DERWENT; IBM_TDB
13	L16	15	13 and 15	EPO; JPO; DERWENT; IBM_TDB
14	L19	13	(vector and instruction and (gather\$3 scatter\$3)).ab,ti.	EPO; JPO; DERWENT; IBM_TDB
15	L20	4	(vector and instruction and (gather\$3 scatter\$3)).ab,ti.	USPAT; US-PGPUB
16	L21	1	(overlap\$4 cover\$3 coincid\$4 match\$3 compar\$3) near20 5 and 4 not 8	USPAT; US-PGPUB
17	L22	1	(overlap\$4 cover\$3 coincid\$4 match\$3 compar\$3) near20 14 and 13 not 16	EPO; JPO; DERWENT; IBM_TDB

	Docum ent ID	U	Title	Current OR
1	US 20030 21706 6 A1	<input type="checkbox"/>	System and methods for character string vector generation	707/100
2	US 20030 21512 7 A1	<input checked="" type="checkbox"/>	Method and system for imaging an object or pattern	382/141
3	US 20030 15871 6 A1	<input checked="" type="checkbox"/>	Procedure for processing measuring data and device to perform the process	703/2
4	US 20020 12879 9 A1	<input checked="" type="checkbox"/>	Method and apparatus for providing predictive maintenance of a device by using markov transition probabilities	702/181
5	US 20020 12877 9 A1	<input checked="" type="checkbox"/>	Seismic imaging using omni-azimuth seismic energy sources and directional sensing	702/14
6	US 20020 11803 4 A1	<input checked="" type="checkbox"/>	Transistor device testing employing virtual device fixturing	324/765
7	US 20020 07234 6 A1	<input checked="" type="checkbox"/>	Method and apparatus for error vector magnitude reduction	455/403
8	US 20020 00744 9 A1	<input checked="" type="checkbox"/>	Vector scatter instruction control circuit and vector architecture information processing equipment	712/4
9	US 66288 44 B1	<input checked="" type="checkbox"/>	High definition imaging apparatus and method	382/276
10	US 66038 74 B1	<input checked="" type="checkbox"/>	Method and system for imaging an object or pattern	382/144
11	US 65533 15 B2	<input checked="" type="checkbox"/>	Seismic imaging using omni-azimuth seismic energy sources and directional sensing	702/14
12	US 65419 93 B2	<input checked="" type="checkbox"/>	Transistor device testing employing virtual device fixturing	324/765
13	US 65298 32 B1	<input checked="" type="checkbox"/>	Seismic imaging using omni-azimuth seismic energy sources and directional sensing	702/6
14	US 64495 66 B1	<input checked="" type="checkbox"/>	Acoustic scattering measurement and processing for determining variances in multiple features	702/54
15	US 64418 21 B1	<input checked="" type="checkbox"/>	Method and apparatus for displaying three-dimensional image by use of tensor rendering	345/426
16	US 64303 07 B1	<input checked="" type="checkbox"/>	Feature extraction system and face image recognition system	382/118
17	US 63962 85 B1	<input checked="" type="checkbox"/>	Method and apparatus for efficient measurement of reciprocal multiport devices in vector network analysis	324/601
18	US 62073 71 B1	<input checked="" type="checkbox"/>	Indexed library of cells containing genomic modifications and methods of making and utilizing the same	435/6
19	US 61987 96 B1	<input checked="" type="checkbox"/>	Method and apparatus of automatically selecting bragg reflections, method and system of automatically determining crystallographic orientation	378/73
20	US 61921 03 B1	<input checked="" type="checkbox"/>	Fitting of X-ray scattering data using evolutionary algorithms	378/73

	Docum ent ID	U	Title	Current OR
21	US 61365 66 A	<input checked="" type="checkbox"/>	Indexed library of cells containing genomic modifications and methods of making and utilizing the same	435/69. 7
22	US 60758 83 A	<input checked="" type="checkbox"/>	Method and system for imaging an object or pattern	382/144
23	US 60347 76 A	<input checked="" type="checkbox"/>	Microroughness-blind optical scattering instrument	356/369
24	US 60236 57 A	<input checked="" type="checkbox"/>	Seismic imaging using omni-azimuth seismic energy sources and directional sensing	702/14
25	US 60164 69 A	<input checked="" type="checkbox"/>	Process for the vector quantization of low bit rate vocoders	704/222
26	US 59012 44 A	<input checked="" type="checkbox"/>	Feature extraction system and face image recognition system	382/190
27	US 58090 43 A	<input checked="" type="checkbox"/>	Method and apparatus for decoding block codes	714/780
28	US 56824 79 A	<input checked="" type="checkbox"/>	System and method for network exploration and access	709/242
29	US 56405 24 A	<input checked="" type="checkbox"/>	Method and apparatus for chaining vector instructions	712/222
30	US 55089 73 A	<input checked="" type="checkbox"/>	Method for determining the principal axes of azimuthal anisotropy from seismic P-wave data	367/38
31	US 54670 83 A	<input checked="" type="checkbox"/>	Wireless downhole electromagnetic data transmission system and method	340/854 .6
32	US 54501 93 A	<input checked="" type="checkbox"/>	Raman spectroscopy of airway gases	356/301
33	US 54266 78 A	<input checked="" type="checkbox"/>	Method for ultrasonic inspection of a closely packed array of fuel rods surrounded by a thin-walled metallic channel	376/252
34	US 51365 50 A	<input checked="" type="checkbox"/>	Method for estimating the residual source of receiver coordinates from CMP gathers	367/38
35	US 49268 68 A	<input checked="" type="checkbox"/>	Method and apparatus for cardiac hemodynamic monitor	600/407
36	US 48497 62 A	<input checked="" type="checkbox"/>	Single-transmission polarization signal extractor	342/188
37	US 48167 67 A	<input checked="" type="checkbox"/>	Vector network analyzer with integral processor	324/601
38	US 46495 06 A	<input checked="" type="checkbox"/>	Vector generator using interpolative analog circuits	708/8
39	US 45485 06 A	<input checked="" type="checkbox"/>	Nondestructive analysis of multilayer roughness correlation	356/446
40	US 45069 79 A	<input checked="" type="checkbox"/>	Compact radiation fringe velocimeter for measuring in three dimensions	356/28. 5
41	US 41722 55 A	<input checked="" type="checkbox"/>	HF coastal current mapping radar system	342/26
42	US 41409 02 A	<input checked="" type="checkbox"/>	Device for measurement of hair-like particulate material	250/225
43	US 41308 07 A	<input checked="" type="checkbox"/>	Feedforward amplifiers	330/124 R

	Docum ent ID	U	Title	Current OR
44	US 37679 29 A	<input type="checkbox"/>	METHOD AND MEANS FOR MEASURING THE ANISOTROPY OF A PLASMA IN A MAGNETIC FIELD	250/366

	Docum ent ID	U	Title	Current OR
1	US 20040 01975 3 A1	<input type="checkbox"/>	System and method for multiple store buffer forwarding in a system with a restrictive memory model	711/154
2	US 20030 18811 1 A1	<input checked="" type="checkbox"/>	Method and apparatus for satisfying load operations	711/154
3	US 20020 18885 2 A1	<input checked="" type="checkbox"/>	Illegal access monitoring device, IC card, and illegal access monitoring method	713/182
4	US 20020 18402 8 A1	<input checked="" type="checkbox"/>	Text to speech synthesizer	704/260
5	US 20020 12919 5 A1	<input checked="" type="checkbox"/>	Microcomputer with built-in programmable nonvolatile memory	711/104
6	US 20020 12081 3 A1	<input checked="" type="checkbox"/>	System and method for multiple store buffer forwarding in a system with a restrictive memory model	711/118
7	US 20020 09352 2 A1	<input checked="" type="checkbox"/>	Methods of encoding and combining integer lists in a computer system, and computer software product for implementing such methods	345/700
8	US 20020 08329 2 A1	<input checked="" type="checkbox"/>	Method of using memory, two dimensional data access memory and operation processing apparatus	711/203
9	US 20020 00744 9 A1	<input checked="" type="checkbox"/>	Vector scatter instruction control circuit and vector architecture information processing equipment	712/4
10	US 20010 05211 4 A1	<input checked="" type="checkbox"/>	Data processing apparatus	717/128
11	US 66970 76 B1	<input checked="" type="checkbox"/>	Method and apparatus for address re-mapping	345/568
12	US 66936 43 B1	<input checked="" type="checkbox"/>	Method and apparatus for color space conversion	345/602
13	US 66788 07 B2	<input checked="" type="checkbox"/>	System and method for multiple store buffer forwarding in a system with a restrictive memory model	711/154
14	US 66779 50 B1	<input checked="" type="checkbox"/>	Graphics computer	345/503
15	US 65909 37 B1	<input checked="" type="checkbox"/>	Efficient motion vector detection	375/240 .16
16	US 65879 16 B2	<input checked="" type="checkbox"/>	Microcomputer with built-in programmable nonvolatile memory	711/103
17	US 65738 46 B1	<input checked="" type="checkbox"/>	Method and apparatus for variable length decoding and encoding of video streams	341/67
18	US 65499 95 B1	<input checked="" type="checkbox"/>	Compressor system memory organization and method for low latency access to uncompressed memory regions	711/202
19	US 65356 19 B1	<input checked="" type="checkbox"/>	Address recognition apparatus and method	382/101

	Docum ent ID	U	Title	Current OR
20	US 64461 57 B1	<input checked="" type="checkbox"/>	Cache bank conflict avoidance and cache collision avoidance	711/5
21	US 62601 57 B1	<input checked="" type="checkbox"/>	Patching of a read only memory	714/8
22	US 61612 08 A	<input checked="" type="checkbox"/>	Storage subsystem including an error correcting cache and means for performing memory to memory transfers	714/764
23	US 61505 98 A	<input checked="" type="checkbox"/>	Tone data making method and device and recording medium	84/603
24	US 61450 55 A	<input checked="" type="checkbox"/>	Cache memory having flags for inhibiting rewrite of replacement algorithm area corresponding to fault cell and information processing system having such a cache memory	711/128
25	US 61417 47 A	<input checked="" type="checkbox"/>	System for store to load forwarding of individual bytes from separate store buffer entries to form a single load word	712/225
26	US 60852 75 A	<input checked="" type="checkbox"/>	Data processing system and method thereof	710/316
27	US 60758 99 A	<input checked="" type="checkbox"/>	Image decoder and image memory overcoming various kinds of delaying factors caused by hardware specifications specific to image memory by improving storing system and reading-out system	382/233
28	US 60584 65 A	<input checked="" type="checkbox"/>	Single-instruction-multiple-data processing in a multimedia signal processor	712/7
29	US 60292 25 A	<input checked="" type="checkbox"/>	Cache bank conflict avoidance and cache collision avoidance	711/5
30	US 59126 71 A	<input checked="" type="checkbox"/>	Methods and apparatus for synthesizing a three-dimensional image signal and producing a two-dimensional visual display therefrom	345/427
31	US 59037 49 A	<input checked="" type="checkbox"/>	Method and apparatus for implementing check instructions that allow for the reuse of memory conflict information if no memory conflict occurs	712/226
32	US 58701 41 A	<input checked="" type="checkbox"/>	Motion vector detection circuit and object tracking camera apparatus	348/169
33	US 58386 94 A	<input checked="" type="checkbox"/>	Dual source data distribution system for integrated circuit tester	714/738
34	US 58225 57 A	<input checked="" type="checkbox"/>	Pipelined data processing device having improved hardware control over an arithmetic operations unit	712/212
35	US 58095 52 A	<input checked="" type="checkbox"/>	Data processing system, memory access device and method including selecting the number of pipeline stages based on pipeline conditions	711/169
36	US 58058 74 A	<input checked="" type="checkbox"/>	Method and apparatus for performing a vector skip instruction in a data processor	712/222
37	US 57897 26 A	<input checked="" type="checkbox"/>	Method and apparatus for enhanced transaction card compression employing interstitial weights	235/380
38	US 57710 47 A	<input checked="" type="checkbox"/>	Graphics computer	345/443
39	US 57548 05 A	<input checked="" type="checkbox"/>	Instruction in a data processing system utilizing extension bits and method therefor	712/200
40	US 57520 74 A	<input checked="" type="checkbox"/>	Data processing system and method thereof	712/29
41	US 57513 64 A	<input checked="" type="checkbox"/>	Method of and apparatus for detecting a motion of image information, method of and apparatus for encoding image information, image information transmitting system, image information recording system and recording medium	375/240 .16

	Document ID	U	Title	Current OR
42	US 5742786 A	<input checked="" type="checkbox"/>	Method and apparatus for storing vector data in multiple non-consecutive locations in a data processor using a mask value	711/217
43	US 5737586 A	<input checked="" type="checkbox"/>	Data processing system and method thereof	712/236
44	US 5734879 A	<input checked="" type="checkbox"/>	Saturation instruction in a data processor	712/221
45	US 5724493 A	<input checked="" type="checkbox"/>	Method and apparatus for extracting 3D information of feature points	345/424
46	US 5717947 A	<input checked="" type="checkbox"/>	Data processing system and method thereof	712/3
47	US 5706488 A	<input checked="" type="checkbox"/>	Data processing system and method thereof	712/223
48	US 5703579 A	<input checked="" type="checkbox"/>	Decoder for compressed digital signals	341/50
49	US 5664134 A	<input checked="" type="checkbox"/>	Data processor for performing a comparison instruction using selective enablement and wired boolean logic	712/245
50	US 5652900 A	<input checked="" type="checkbox"/>	Data processor having 2n bits width data bus for context switching function	718/100
51	US 5619713 A	<input checked="" type="checkbox"/>	Apparatus for realigning database fields through the use of a crosspoint switch	707/102
52	US 5600846 A	<input checked="" type="checkbox"/>	Data processing system and method thereof	712/5
53	US 5598571 A	<input checked="" type="checkbox"/>	Data processor for conditionally modifying extension bits in response to data processing instruction execution	712/9
54	US 5592613 A	<input checked="" type="checkbox"/>	Microcomputer having a program correction function	714/6
55	US 5590362 A	<input checked="" type="checkbox"/>	Database engine predicate evaluator	707/4
56	US 5572689 A	<input checked="" type="checkbox"/>	Data processing system and method thereof	712/200
57	US 5566303 A	<input checked="" type="checkbox"/>	Microcomputer with multiple CPU'S on a single chip with provision for testing and emulation of sub CPU's	710/100
58	US 5560036 A	<input checked="" type="checkbox"/>	Data processing having incircuit emulation function	712/227
59	US 5559973 A	<input checked="" type="checkbox"/>	Data processing system and method thereof	712/241
60	US 5548769 A	<input checked="" type="checkbox"/>	Database engine	707/1
61	US 5548768 A	<input checked="" type="checkbox"/>	Data processing system and method thereof	712/200
62	US 5548739 A	<input checked="" type="checkbox"/>	Method and apparatus for rapidly retrieving data from a physically addressed data storage structure using address page crossing predictive annotations	711/204
63	US 5537622 A	<input checked="" type="checkbox"/>	Database engine	707/1
64	US 5537604 A	<input checked="" type="checkbox"/>	Database engine	707/1

	Docum ent ID	U	Title	Current OR
65	US 55376 03 A	<input checked="" type="checkbox"/>	Database engine	707/1
66	US 55375 62 A	<input checked="" type="checkbox"/>	Data processing system and method thereof	712/234
67	US 55308 83 A	<input checked="" type="checkbox"/>	Database engine	712/18
68	US 54817 34 A	<input checked="" type="checkbox"/>	Data processor having 2n bits width data bus for context switching function	712/225
69	US 54407 57 A	<input checked="" type="checkbox"/>	Data processor having multistage store buffer for processing exceptions	712/228
70	US 54189 73 A	<input checked="" type="checkbox"/>	Digital computer system with cache controller coordinating both vector and scalar operations	712/3
71	US 53715 39 A	<input checked="" type="checkbox"/>	Video camera with electronic picture stabilizer	348/208 .6
72	US 53596 97 A	<input checked="" type="checkbox"/>	Fuzzy associative memory	706/1
73	US 53576 27 A	<input checked="" type="checkbox"/>	Microcomputer having a program correction function	714/6
74	US 53496 92 A	<input checked="" type="checkbox"/>	Instruction handling sequence control system for simultaneous execution of vector instructions	712/9
75	US 53255 10 A	<input checked="" type="checkbox"/>	Multiprocessor system and architecture with a computation system for minimizing duplicate read requests	711/118
76	US 52874 98 A	<input checked="" type="checkbox"/>	Message transmitting system wherein recipient site is determined using information concerning the relationship between the sender and recipient sites	707/10
77	US 52631 68 A	<input checked="" type="checkbox"/>	Circuitry for automatically entering and terminating an initialization mode in a data processing system in response to a control signal	713/1
78	US 52631 44 A	<input checked="" type="checkbox"/>	Method and apparatus for sharing data between processors in a computer system	711/121
79	US 52476 35 A	<input checked="" type="checkbox"/>	Vector processing system for invalidating scalar cache memory block indicated by address in tentative vector store instruction	711/3
80	US 52416 33 A	<input checked="" type="checkbox"/>	Instruction handling sequence control system for simultaneous execution of instructions	712/216
81	US 52186 80 A	<input checked="" type="checkbox"/>	Data link controller with autonomous in tandem pipeline circuit elements relative to network channels for transferring multitasking data in cyclically recurrent time slots	709/215
82	US 52108 70 A	<input checked="" type="checkbox"/>	Database sort and merge apparatus with multiple memory arrays having alternating access	707/7
83	US 52069 33 A	<input checked="" type="checkbox"/>	Data link controller with channels selectively allocatable to hyper channels and hyper channel data funneled through reference logical channels	709/250
84	US 51828 11 A	<input checked="" type="checkbox"/>	Exception, interrupt, and trap handling apparatus which fetches addressing and context data using a single instruction following an interrupt	710/264
85	US 51213 90 A	<input checked="" type="checkbox"/>	Integrated data link controller with synchronous link interface and asynchronous host processor interface	370/458
86	US 50104 83 A	<input checked="" type="checkbox"/>	Vector processor capable of indirect addressing	712/6



	Docum ent ID	U	Title	Current OR
87	US 49790 39 A	<input checked="" type="checkbox"/>	Method and apparatus for vector quantization by hashing	375/240 22
88	US 49033 17 A	<input checked="" type="checkbox"/>	Image processing apparatus	382/244
89	US 48736 30 A	<input checked="" type="checkbox"/>	Scientific processor to support a host processor referencing common memory	712/3
90	US 48705 69 A	<input checked="" type="checkbox"/>	Vector access control system	711/151
91	US 47991 86 A	<input checked="" type="checkbox"/>	Electronic circuit constituting an improved high-speed stable memory with memory zones protect from overlap	711/152
92	US 47808 10 A	<input checked="" type="checkbox"/>	Data processor with associative memory storing vector elements for vector conversion	712/6
93	US 47697 70 A	<input checked="" type="checkbox"/>	Address conversion for a multiprocessor system having scalar and vector processors	711/206
94	US 47348 77 A	<input checked="" type="checkbox"/>	Vector processing system	708/441
95	US 47208 64 A	<input checked="" type="checkbox"/>	Speech recognition apparatus	704/241
96	US 45354 19 A	<input checked="" type="checkbox"/>	System and method for computing fractional postage values	705/407
97	US 44583 30 A	<input checked="" type="checkbox"/>	Banded vector to raster converter	345/501
98	US 43756 54 A	<input checked="" type="checkbox"/>	Facsimile vector data compression	382/199
99	US 42863 25 A	<input checked="" type="checkbox"/>	System and method for computing domestic and international postage	705/402
100	US 39064 80 A	<input checked="" type="checkbox"/>	Digital television display system employing coded vector graphics	345/17
101	US 38953 57 A	<input checked="" type="checkbox"/>	Buffer memory arrangement for a digital television display system	345/559
102	US 38837 28 A	<input type="checkbox"/>	Digital vector generator	708/168

	Docum ent ID	U	Title	Current OR
1	JP 20023 66538 A	<input type="checkbox"/>	VECTOR PROCESSOR AND PASSING CONTROL METHOD USING THE SAME	
2	JP 20020 24205 A	<input checked="" type="checkbox"/>	VECTOR SCATTER INSTRUCTION CONTROL CIRCUIT AND VECTOR TYPE INFORMATION PROCESSOR	
3	JP 20011 95389 A	<input checked="" type="checkbox"/>	BOUNDARY EXECUTION CONTROLLER AND BOUNDARY CONTROL METHOD	
4	JP 11065 856 A	<input checked="" type="checkbox"/>	MICROCOMPUTER AND ITS INTERRUPTION PROCESSING METHOD	
5	JP 09034 878 A	<input checked="" type="checkbox"/>	VECTOR REGISTER SYSTEM	
6	JP 02254 563 A	<input checked="" type="checkbox"/>	VECTOR DATA PROCESSING SYSTEM	
7	JP 02110 668 A	<input checked="" type="checkbox"/>	BUFFER STORAGE CONTROLLER	
8	JP 02085 960 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSING SYSTEM	
9	JP 01054 542 A	<input checked="" type="checkbox"/>	VIRTUAL COMPUTER SYSTEM	
10	JP 61296 472 A	<input checked="" type="checkbox"/>	BUFFER MEMORY DEVICE	
11	EP 11727 25 A2	<input checked="" type="checkbox"/>	Vector scatter instruction control circuit and vector architecture information processing equipment	
12	EP 39689 2 A2	<input checked="" type="checkbox"/>	Data processing apparatus.	
13	EP 11727 25 A	<input checked="" type="checkbox"/>	Vector scatter instruction control circuit in vector architecture information processor, holds following memory access instruction, if address specified by vector scatter instruction overlaps with following instruction address	
14	JP 11065 856 A	<input checked="" type="checkbox"/>	Branch address accessing mechanism of microcomputer - accesses second branch address, based on program stored in readable area of EPROM, when coincidence of first branch address with first specific value is conformed according to input interruption signal	
15	EP 39689 2 A	<input type="checkbox"/>	Data processing appts. nulling scalar cache memory - according to vector store instruction via instruction passing issuing control before vector store instruction	

	Docum ent ID	U	Title	Current OR
1	JP 20020 24205 A	<input type="checkbox"/>	VECTOR SCATTER INSTRUCTION CONTROL CIRCUIT AND VECTOR TYPE INFORMATION PROCESSOR	
2	JP 05342 105 A	<input checked="" type="checkbox"/>	CACHE INVALIDATION PROCESSOR	
3	JP 01032 378 A	<input checked="" type="checkbox"/>	BIT INVERTING AND TRANSPOSING SYSTEM	
4	JP 63285 668 A	<input checked="" type="checkbox"/>	VECTOR LOAD PROCESSING METHOD	
5	JP 62001 067 A	<input checked="" type="checkbox"/>	VECTOR PROCESSOR	
6	JP 60136 874 A	<input checked="" type="checkbox"/>	VECTOR PROCESSOR	
7	JP 60065 333 A	<input checked="" type="checkbox"/>	LOGICAL DEVICE	
8	JP 59125 455 A	<input checked="" type="checkbox"/>	GENERATING METHOD OF TEST DATA	
9	EP 11727 25 A2	<input checked="" type="checkbox"/>	Vector scatter instruction control circuit and vector architecture information processing equipment	
10	EP 11071 17 A2	<input checked="" type="checkbox"/>	Concurrent legacy and native code execution techniques	
11	EP 11727 25 A	<input checked="" type="checkbox"/>	Vector scatter instruction control circuit in vector architecture information processor, holds following memory access instruction, if address specified by vector scatter instruction overlaps with following instruction address	
12	US 56405 24 A	<input checked="" type="checkbox"/>	High performance scalar and vector processor for supercomputer - has instruction processor reading vector words from elements of vector register filled according to instruction request unit	
13	EP 35886 3 A	<input type="checkbox"/>	Data block reading method for multiprocessor system - providing mechanism for controlling CPU to use appropriate command to load data depending on whether vector will be written	